WHAT IS CLAIMED IS

1. A semiconductor memory device, comprising:

a memory cell;

a signal line on which a potential responsive to data read from said memory cell appears;

a potential detecting circuit which outputs a detection signal in response to detecting that the potential on said signal line exceeds a predetermined potential; and

a sense amplifier which starts amplifying the potential on said signal line in response to the detection signal.

2. The semiconductor memory device as claimed in claim 1, wherein said memory cell includes two ferroelectric capacitors for storing complementary data, and said signal line includes two signal lines corresponding to said two ferroelectric capacitors, and wherein said potential detecting circuit includes two potential detecting circuits provided for respective ones of said two signal lines, and said sense amplifier starts amplifying data on said two signal lines when either one of said two potential detecting circuits outputs the detection signal.

3. The semiconductor memory device as claimed in claim 1, further comprising:

a bit line on which a potential responsive to the data read from said memory cell appears; and

a pre-sense amplifier which amplifies the potential on said bit line for provision to said signal line.

4. The semiconductor memory device as claimed in claim 1, wherein said potential detecting circuit is a Schmitt trigger circuit.

5. The semiconductor memory device as claimed in claim 4, wherein an input-and-output characteristic of said Schmitt trigger circuit with respect to an input positive transition is identical to an input-and-output characteristic of an inverter that includes a Pch-MOS transistor and an Nch-MOS transistor connected in series.

6. The semiconductor memory device as claimed in claim 1, further comprising a delay circuit which delays the detection signal output from said potential detecting circuit for provision to said sense amplifier.

7. A semiconductor memory device, comprising:

a memory cell which includes two ferroelectric capacitors for storing complementary data;

two bit lines each connected to a corresponding one of said two ferroelectric capacitors through a transistor;

two pre-sense amplifiers each coupled to a corresponding one of said two bit lines for amplifying a potential;

two potential detecting circuits each coupled to an output of a corresponding one of said two pre-sense amplifiers to output a detection signal in response to detecting that the output of the corresponding one of said two pre-sense amplifiers exceeds a predetermined potential; and

a sense amplifier coupled to outputs of said two pre-sense amplifiers to start amplification in response to the detection signal that is output from either one of said two potential detecting circuits.

8. The semiconductor memory device as claimed in claim 7, wherein said potential detecting circuit is a Schmitt trigger circuit.

9. The semiconductor memory device as claimed in claim 8, wherein an input-and-output

characteristic of said Schmitt trigger circuit with respect to an input positive transition is identical to an input-and-output characteristic of an inverter that includes a Pch-MOS transistor and an Nch-MOS transistor connected in series.

10. The semiconductor memory device as claimed in claim 7, further comprising a delay circuit which delays the detection signal output from said potential detecting circuit for provision to said sense amplifier.